

What is claimed is:

- 1 1. A method comprising:
2 setting a first indicator; and
3 interrupting execution of a computer program instruction in response to
4 setting the first indicator.
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- 1 2. The method of claim 1, further comprising:
2 setting a second indicator; and
3 halting execution of the computer program instruction in response to setting
4 the first and second indicators.
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- 1 3. The method of claim 2, further comprising:
2 resetting the first indicator; and
3 resuming execution of the computer program instruction in response to
4 resetting the first indicator.
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- 1 4. The method of claim 2, wherein the first and second indicators comprise
2 data bits.
3
- 1 5. The method of claim 4, wherein the data bits are held in a register.
2
- 1 6. The method of claim 1, further comprising:
2 setting a second indicator;
3 setting a third indicator; and
4 halting execution of the computer program instruction in response to setting
5 the second and third indicators.
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- 1 7. The method of claim 6, further comprising:
2 resetting the third indicator; and

3 resuming execution of the computer program instruction in response to
4 resetting the third indicator.

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1 8. The method of claim 6, wherein the computer program instruction includes
2 the first indicator.

3

1 9. The method of claim 6, wherein the second and third indicators comprise
2 data bits.

3

1 10. The method of claim 9, wherein the data bits are held in a register.

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1 11. The method of claim 1, further comprising:
2 resetting the first indicator;
3 setting a second indicator; and
4 halting execution of the computer program instruction in response to
5 resetting the first indicator and setting the second indicator.

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1 12. The method of claim 11, further comprising:
2 resetting the second indicator; and
3 resuming execution of the computer program instruction in response to
4 resetting the second indicator.

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1 13. The method of claim 11, further comprising:
2 setting the first indicator;
3 resetting the second indicator;
4 resuming execution of the computer program instruction in response to
5 setting the first indicator and to resetting the second indicator; and
6 interrupting execution of a subsequent computer program instruction in
7 response to setting the first indicator and to resetting the second indicator.

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- 1 14. The method of claim 13, further comprising:
2 resetting the first indicator;
3 setting the second indicator; and
4 halting execution of the subsequent computer program instruction in
5 response to resetting the first indicator and to setting the second indicator.
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- 1 15. The method of claim 11, wherein the first and second indicators comprise
2 data bits.
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- 1 16. The method of claim 15, wherein the data bits are held in a register.
2
- 1 17. An apparatus comprising:
2 a processor; and
3 at least one indicator coupled to the processor, wherein the at least one
4 indicator is configurable to halt execution of a computer program instruction by the
5 processor.
6
- 1 18. The apparatus of claim 17, wherein the at least one indicator comprises at
2 least one data bit readable by the processor.
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- 1 19. The apparatus of claim 18, wherein the at least one data bit is held in a
2 register coupled to the processor.
3
- 1 20. The apparatus of claim 17, wherein the computer program instruction
2 executed by the processor includes at least one indicator configurable to interrupt
3 execution of the computer program instruction.
4
- 1 21. The apparatus of claim 20, wherein the at least one indicator included in the
2 computer instruction comprises at least one data bit.
3

- 1 22. The apparatus of claim 17 wherein the at least one indicator is
2 reconfigurable to resume execution of the computer program instruction.
3
- 1 23. The apparatus of claim 17 wherein the at least one indicator is
2 reconfigurable to resume execution of the computer program instruction and to halt
3 execution of a subsequent computer program by the processor.
4
- 1 24. A machine-readable medium that provides instructions, which when
2 executed by a machine, cause said machine to perform operations comprising:
3 configuring at least one indicator coupled to a processor;
4 halting execution by the processor of an instruction issued by a computer
5 program in response to the configuring of the at least one indicator;
6 reconfiguring the at least one indicator; and
7 finishing execution by the processor of the instruction issued by the
8 computer program in response to the reconfiguring of the at least one indicator.
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- 1 25. The machine-readable medium of claim 24, wherein the at least one
2 indicator comprises at least one data bit.
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- 1 26. The machine-readable medium of claim 25, wherein the at least one data bit
2 is held in a register coupled to the processor.
3
- 1 27. The machine-readable medium of claim 24, wherein the at least one
2 indicator comprises at least one indicator included in the computer program
3 instruction, wherein the at least one indicator included in the computer program
4 instruction is configurable to interrupt execution of the computer program
5 instruction.
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1 28. The machine-readable medium of claim 27, wherein the at least one
2 indicator included in the computer program instruction comprises at least one data
3 bit.

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1 29. The machine-readable medium of claim 24, wherein reconfiguring the at
2 least one indicator causes the processor to halt execution of a subsequent computer
3 program instruction.

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1 30. A system comprising:
2 a processor to execute computer program instructions;
3 a memory coupled to the processor, the memory to store the computer
4 program instructions to be executed by the processor; and
5 at least one indicator coupled to the processor, the at least one indicator
6 configurable to control execution of the computer program instructions by the
7 processor.

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1 31. The system of claim 30, wherein the at least one indicator comprise at least
2 one data bit configurable to halt execution of one or more of the computer program
3 instructions by the processor.

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1 32. The system of claim 31, wherein the at least one data bit is reconfigurable to
2 resume execution of the one or more of the computer program instructions by the
3 processor.

4

1 33. The system of claim 30, wherein the at least one indicator comprises at least
2 one data bit.

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1 34. The system of claim 33, wherein the at least one data bit is held in a register.

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1 35. The system of claim 30, wherein the at least one indicator comprises at least
2 one indicator included in the computer program instruction, wherein the at least one
3 indicator included in the computer program instruction is configurable to interrupt
4 execution of the computer program instruction.

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1 36. The system of claim 35, wherein the at least one indicator included in the
2 computer program instruction comprises at least one data bit.

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1 37. An apparatus comprising:
2 at least one indicator configurable to halt execution of a computer program
3 instruction by embedded logic.

4

1 38. The apparatus of claim 37, wherein the at least one indicator is at least one
2 data bit readable by embedded logic.

3

1 39. The apparatus of claim 38, wherein the at least one data bit is held in a
2 register.

3

1 40. The apparatus of claim 37, wherein the computer program instruction
2 executable by embedded logic includes at least one indicator configurable to
3 interrupt execution of the computer program instruction.

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1 41. The apparatus of claim 40, wherein the at least one indicator included in the
2 computer instruction comprises at least one data bit.

3

1 42. The apparatus of claim 37, wherein the at least one indicator is
2 reconfigurable to resume execution of the computer program instruction.

3

1 43. The apparatus of claim 37, wherein the at least one indicator is
2 reconfigurable to resume execution of the computer program instruction and to halt
3 execution of a subsequent computer program.
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1 44. A machine-readable medium that provides instructions, which when
2 executed by a machine, cause said machine to perform operations comprising:
3 configuring at least one indicator readable by embedded logic;
4 halting execution by embedded logic of an instruction issued by a computer
5 program in response to the configuring of the at least one indicator;
6 reconfiguring the at least one indicator; and
7 finishing execution by embedded logic of the computer program instruction
8 in response to the reconfiguring of the at least one indicator.
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1 45. The machine-readable medium of claim 44, wherein the at least one
2 indicator comprises at least one data bit.
3

1 46. The machine-readable medium of claim 45, wherein the at least one data bit
2 is held in a register.
3

1 47. The machine-readable medium of claim 44, wherein the at least one
2 indicator comprises at least one indicator included in the computer program
3 instruction, wherein the at least one indicator included in the computer program
4 instruction is configurable to interrupt execution of the instruction.
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1 48. The machine-readable medium of claim 47, wherein the at least one
2 indicator included in the computer program instruction comprises at least one data
3 bit.
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- 1 49. The machine-readable medium of claim 44, wherein embedded logic halts
2 execution of a subsequent computer program instruction in response to
3 reconfiguring the at least one indicator.
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- 1 50. A system comprising:
2 computer program instructions executable by embedded logic;
3 a memory to store the computer program instructions; and
4 at least one indicator configurable to control execution of the computer
5 program instructions.
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- 1 51. The system of claim 50, wherein the at least one indicator comprises at least
2 one data bit configurable to halt execution of one or more of the computer program
3 instructions.
4
- 1 52. The system of claim 51, wherein the at least one data bit is reconfigurable to
2 resume execution of the one or more of the computer program instructions.
3
- 1 53. The system of claim 50, wherein the at least one indicator comprises at least
2 one indicator included in the computer program instruction, wherein the at least one
3 indicator included in the computer program instruction is configurable to interrupt
4 execution of the instruction.
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- 1 54. The system of claim 53, wherein the at least one indicator included in the
2 computer program instruction comprises at least one data bit.
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- 1 55. The system of claim 50, wherein at least one indicator comprises at least one
2 data bit.
3
- 1 56. The system of claim 55, wherein the at least one data bit is held in a register.
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